Customer No.: 31561
Application No.: 10/707,082
Docket No.: 11690-US-PA

REMARKS

Present Status of the Application

Claims 1-11 remain pending of which claim 5 has been amended to correct a minor typographical error. It is believed that no new matter adds by way of amendments made to the claims or otherwise to the application. For at least the following reasons, Applicant respectfully submits that claims 1-11 are in proper condition for allowance. Reconsideration is respectfully requested.

Discussion of the claim rejection under 35 USC 102

The Office Action rejected claims 1, 2, 5 and 7 under 35 U.S.C. 102(e) as being anticipated by Sakimura et al. (US-6,885,579, hereinafter Sakimura).

Applicants respectfully disagree and submit that it is well established that under 35 U.S.C. 102, each and every elements of the rejected claim must be exactly disclosed by a single prior art reference.

Independent claim 1, as amended, is allowable over Sakimura for at least the reason that Sakimura substantially fails to teach or disclose each and every features of the claimed invention. More specifically, Sakimura cannot anticipate the amended proposed independent claim 1 because Sakimura substantially fails to teach or disclose [a device for breaking a leakage current path in a memory array comprising at least a switch device coupled to the memory cell, a power supply terminal, the column selection line and the row selection line, wherein when the column selection line receives a column turn-off signal and the row selection line receives a row turn-off signal, the switch device is turned off so that a power provided from the power supply terminal is not coupled to the memory cell, and when at least one of the column selection line and the row selection line

does not receive at least one of the column turn-off signal and the row turn-off signal, the power provided from the power supply terminal is coupled to the memory cell] as required by the proposed independent claim 1. The advantage of the above features is that at least not only the problems due to current leakage in the memory cell are resolved but also reduction of service life of the batteries, slowing down of operating speed of the memory devices, increase in operating temperature of the computer.

Instead, Sakimura substantially teaches that parasitic electric current (or sneak path electric current) in a MRAM damages the reliability of determination of data stored in a memory cell in a MRAM adopting a cross point cell array. According to Sakimura, the sneak path electric current hinders the correct detection of the resistance of the memory cell when the data stored in the memory cell is determined (please see col. 1, line 66 to col. 2, line 8). In order to resolve this problem, Sakimura, at FIG. 4, col. 14, lines 5-67, substantially teaches determining the difference Is-Ic between the detection electric current Is and the offset component electric current Ic by subtracting an offset component from the detection electric current Is and removing the component depending on the sneak path electric current from the electric current Is-Ic so that an influence of the sneak path electric current is restrained, by determining the data stored in the selected memory cell 2a based on the electric current Is-Ic. According to Sakimura, the offset component mainly contains an electric current component generated based on the sneak path electric current and an electric current component based on the resistance component R.

Accordingly, Applicants respectfully submit that the objective and the purpose of Sakimura is also substantially different from the claimed invention, in that Sakimura

substantially teaches a scheme of determining correct resistance of the memory cell for determining the correct data stored in the memory cell, while the present inventors propose breaking the current leakage path by breaking the power supply to the defective memory cells using a switch device coupled to the memory cell, a power supply terminal, the column selection line and the row selection line, wherein when the column selection line receives a column turn-off signal and the row selection line receives a row turn-off signal, the switch device is turned off so that a power provided from the power supply terminal is not coupled to the memory cell, and when at least one of the column selection line and the row selection line does not receive at least one of the column turn-off signal and the row turn-off signal, the power provided from the power supply terminal is coupled to the memory cell, as claimed in the proposed independent claim 1, in order to eliminate or reduce problems due to current leakage of the defective memory cells, for example, reduction of service life of the batteries, slowing down of operating speed of the memory devices, increase in operating temperature of the computer. In other words, Sakimura substantially teaches away from the claimed invention in this regard.

Therefore, Applicants respectfully submit that Sakimura cannot possibly anticipate the amended proposed independent claim 1 in this regard.

Because the proposed independent claims 5 and 7, as amended, also recite features that are similar to the amended proposed independent claim 1, therefore Applicants similarly submit that claims 5 and 7 also patently defines over Sakimura for at least the same reasons discussed above.

Claims 2, which directly depend from the independent 1 Claim is also patentable over Sakimura at least because of their dependency from an allowable base claim.

For at least the foregoing reasons, Applicants respectfully submit that claims 1, 2, 5 and 7 patently define over Sakimura. Reconsideration and withdrawal of above rejections is respectfully requested.

Discussion of the claim rejection under 35 USC 103

1. The Office Action rejected claims 4, 6, 10 and 11 under 35 U.S.C. 103(a) as being unpatentable over Sakimura in view Arimoto et al. (US-2003/0103368, hereinafter Arimoto).

Applicants respectfully disagree and would like to point out that Arimoto substantially teaches a configuration in which a bit line precharge/equalize circuit is arranged in a sense amplifier band, a standby current can be likewise detected by disconnecting all non-selected memory cell arrays (memory blocks) from sense amplifier bands. In the sleep mode, by disconnecting a leakage-defective memory cell array from sense amplifier bands, a consumed current can be reduced even in a configuration in which a bit line precharge/equalize circuit is arranged in a sense amplifier band. As a configuration for control in such an arrangement, the configuration of control described above can be utilized. In other words, because Arimoto substantially fails to teach, suggest or hint disconnecting the power supply to the selected defective memory cell, instead Arimoto substantially teaches disconnecting a leakage-defective memory cell array from sense amplifier bands. Accordingly, even if the above features of the Arimoto were to be incorporated into Sakimura in a manner suggested by the Examiner, still the

combination cannot possibly render every features of the claimed invention for at least the reasons discussed above.

For at least the foregoing reasons, Applicants respectfully submit that claims 4, 6, 10 and 11 patently define over Sakimura and Arimoto. Reconsideration and withdrawal of above rejections is respectfully requested.

2. The Office Action rejected claims 3 and 9 under 35 U.S.C. 103(a) as being unpatentable over Sakimura in view of Marr et al. (US-6,707,707, hereinafter Marr).

Applicants respectfully disagree and submit that the PMOS transistor or PMOSFET transistor of Marr still cannot cure the specific deficiencies of Sakimura for at least the reasons substantially discussed above. Accordingly, Applicants respectfully submit that no combination of Sakimura and Marr in a manner suggested by the Examiner could possibly render every features of the claimed invention in this regard.

For at least the foregoing reasons, Applicants respectfully submit that claims 3 and 9 patently define over Sakimura and Marr. Reconsideration and withdrawal of above rejections is respectfully requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-11 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

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